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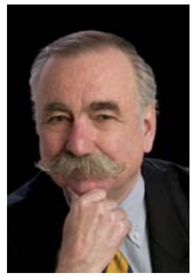
EDA to the Rescue of the Silicon Roadmap



Dr. THOMAS W. WILLIAMS
Synopsys Fellow
Synopsys, Inc.

Since the invention of the transistor nearly six decades ago, new technology nodes have been added approximately every two years. This march of progress has yielded smaller transistors that run about 40% faster with each geometry scaling, fulfilling the promise and industry-defining mantra of "smaller, faster, cheaper!" Now, in the realm of 65- and 45-nanometer design and manufacturing, the industry is confronted by multiple complex and stubborn challenges: silicon technology keeps shrinking, but doesn't advance in speed at the same rate. The recent high-k dielectric announcements have yet to be proven manufacturable, and copper interconnect is already hitting the wall. We are driving to the edge of the silicon roadmap, but there is no viable alternative to CMOS within our reach. Not coincidentally, several companies are announcing their intention to stop internal R&D at the 45 nanometer node and use foundry-supplied processes at 32 nanometers and below. The electronics industry ecosystem is at a fork in the road: those few who can afford it will keep rushing to 45 nanometers and maybe beyond, to 32 and 25 nanometers; the rest will hold at 130 or perhaps 90 nanometers, trying to get the most out of those processes that they can. In both cases it is EDA that will come to the rescue. Advanced EDA provides a competitive advantage at 90 nanometers and above, and is a matter of plain survival at 65 nanometers and below. In 2006 only 10% of IC design starts have been at 90 nanometers and below (source: IBS), but they have generated more than 30% of silicon (source: VLSI Research), and absorbed more than 50% of all the engineering effort (source: SNUG '06). Without EDA, more EDA, or more advanced EDA, when design starts at 90 nanometers and below exceed 30% in 2 years (source: IBS), twice as many engineers will be needed. EDA innovation is the gear that enables design for low power, design for manufacturing and yield (which encompasses design for test), and design for variability. The challenges faced by tools for Multiple-Valued Logic clearly mirror those challenges faced by binary logic EDA tools. EDA is not only the enabler for quality in electronic design; it is truly "where electronics begins!"

BIOGRAPHY

Dr. Thomas W. Williams is a Synopsys Fellow at Synopsys in Boulder, Colorado, U.S.A. Formerly, he was with IBM Microelectronics Division and manager of the VLSI Design for Testability group. He received a B.S.E.E. from Clarkson University, an M.A. in pure mathematics from the State University of New York at Binghamton, and a Ph.D. in electrical engineering from Colorado State University. He has received numerous best paper awards from the IEEE and ACM, is the founder or co-founder of a number of workshops and conferences dealing with testing, and was twice a Distinguished Visitor lecturer for the IEEE Computer Society. Dr. Williams has previously served on the Computer Society Board of Governors and the IEEE Board of Directors, and was the Society's 2000 Treasurer. He is a member of the Eta Kappa Nu, Tau Beta Pi, IEEE, ACM, Sigma Xi, and Phi Kappa Phi. He is an Adjunct Professor at the University of Calgary, Calgary, Alberta, Canada; and in 1985 and 1997, he was a Guest Professor and Robert Bosch Fellow at the Universitaet of Hannover, Hannover, Germany. Dr. Williams was named an IEEE Fellow in 1988 and received the Computer Society's W. Wallace McDowell Award for outstanding contributions to the computer art in 1989. He was named a member of the Chinese Academy of Science in 2007. In 2007 Dr. Williams received the European Design and Automation Association Lifetime Achievement Award for "outstanding contributions to the state of the art in electronic design, automation, and testing of electronic systems."