
EE5321/EE7321

Semiconductor Devices and Circuits

MOS Models

MOS Models: Motivation

- Modeling is an enabler for circuit analysis and design.
 - Simplify the description of system components.
- Examples:
 - A group of components (transistors, capacitor, resistors) can be represented by a "model"
 - An Operational Amplifier (Op Amp)
 - A current source
 - A component can be represented by a "model"
 - Description of a transistor by a group of capacitors, resistors and controlled sources

MOS Models: Quest for a linear description

- Electronic devices have, in general, 3 or more terminals.
 - The voltage-current relationships among terminals are usually non-linear
- The design and analysis of non-linear systems is an extremely complex task.
- There is a need for simple linear models to describe the electronic devices. In particular, transistors.

MOS Models: Large and Small signal models

- Transistor modeling is divided in two categories:
 - Large-signal models
 - Small-signal models
- Large-signal models represent the non-linear behavior of the electronic device
- Small-signal models describe the current-voltage between terminals using linear relationships.
 - This is accomplished by limiting the signal amplitudes to a range where the linear descriptions are valid.

MOS Models: Caveat

- Always keep in mind that models are a simplified description of the device.
 - The analysis and design will be as accurate as the model used.
- **WARNING:** A simulator relies on models to perform a circuit analysis.
 - It is not unusual that a circuit presents a different "real life" behavior compared to the modeled/simulated result.
 - An important challenge is to find the discrepancies and/or missing parts of the models used in the simulator to match the real data.

MOS Models: Device Operation 1

- The Metal-Oxide-Semiconductor (MOS) transistor is a voltage controlled current switch, where the gate voltage controls the current flow between source and drain.
- Typical symbols used to represent MOS transistors are:

NMOSFET

PMOSFET

MOS Models: Device Operation 2

- Notice: The MOS transistor is a 4 terminal device.
- The Body contact (also known as: bulk or substrate) is biased to ensure that the junctions at the source and drain regions are reverse biased.
 - This means that:
 - In NMOS the body is tied to the lowest potential, which is usually the ground. The body in NMOS is a p⁻ region.
 - In PMOS the body is tied to the highest potential, which is usually V_{DD} . The body in PMOS is an n⁻ region.
 - These connections are assumed, unless specified otherwise.

MOS Models: The MOS capacitor

- The NMOSFET will be the main vehicle for our modeling.
- The MOS capacitor is a key component of the MOS transistor.
 - Actually, MOS devices only became viable after the issues of producing MOS capacitors have been solved.
- For the analysis of the MOS capacitor we will tie the source, drain and body of an NMOSFET to ground. We will investigate the impact of the gate bias on the MOS structure.

MOS Models: MOS Cap accumulation

- MOS Capacitor with $V_{GS} \ll 0$
 - Holes are attracted to and accumulate at the gate oxide to substrate interface.
 - The device can be described as a capacitor with unit area of C_{ox} as the two "plates" of the capacitor are separated by the gate oxide with thickness t_{ox} .
 - C_{ox} is the gate capacitance per unit area, given by:

$$C_{ox} = \frac{K_{ox} \cdot \epsilon_0}{t_{ox}}$$

where $K_{ox} = 3.9$ is the relative permittivity of SiO_2 and

$\epsilon_0 = 8.854 \times 10^{-12}$ F/m is the permittivity of free space.

MOS Models: MOS Cap depletion

- MOS capacitor with $V_{FB} < V_{GS} < V_{TH}$
 - This is a transition region.
 - The device moves:
 - From having a layer of holes accumulated at the interface between the gate oxide and substrate.
 - Towards having a layer of electrons piled at this very same interface.
 - During the transition a depletion region is formed in the substrate under the MOS capacitor.
 - The device is described by the series combination of the C_{ox} and $C_{depletion}$ capacitances.
 - As the depletion regions width varies with V_{GS} , also $C_{depletion}$ and the total MOS capacitance varies.

MOS Models: MOS Cap V_{FB} and V_{TH}

- V_{FB} and V_{TH} are the voltages that define the MOS capacitor transition points.
- The flatband voltage (V_{FB}) is defined where there is no accumulated holes at the interface and the device starts to develop a depletion region in the substrate.
- The threshold voltage (V_{TH}) is defined where a significant inversion layer is present at the interface between the gate oxide and the substrate. At this point a channel connecting source and drain is considered to exist.

MOS Models: MOS Cap inversion

- MOS capacitor with $V_{GS} > V_{TH}$
- Electrons pile at the interface between the gate oxide and the substrate where they create an inversion layer.
- This layer of charge shields the depletion region from the gate electrode.
- The device can be described as a capacitor with an unit area capacitance of C_{ox} .

MOS Models: MOS drawings

- Accumulation

$$V_{GS} \ll 0$$

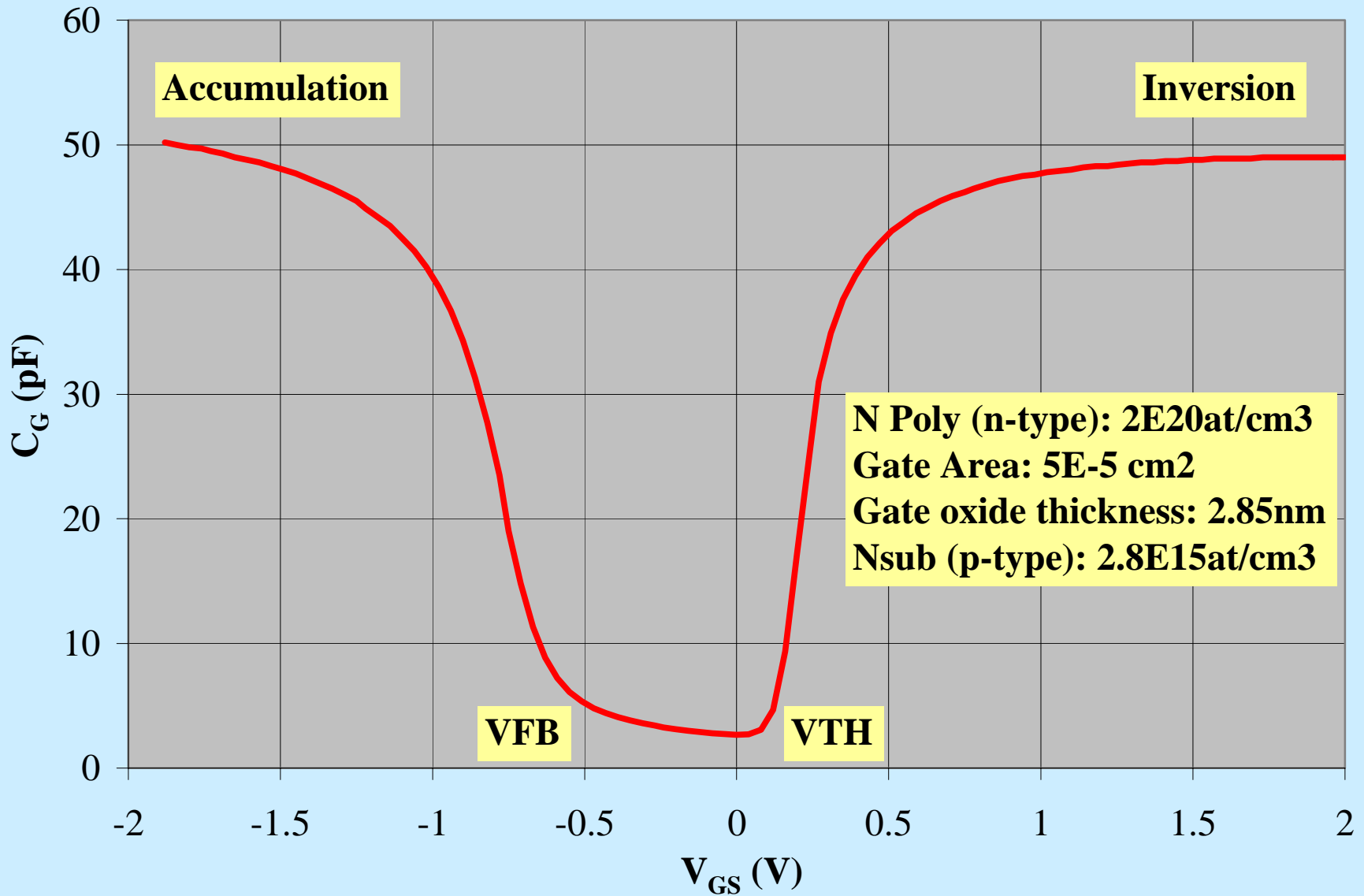
- Transition

$$V_{FB} < V_{GS} < V_{TH}$$

- Inversion

$$V_{GS} > V_{TH}$$

MOS Models: Typical MOS Cap curve



MOS Models: MOS Cap 2nd order effects

- Polysilicon gate electrodes are heavily doped ($1E20\text{at}/\text{cm}^3$).
- However, there is a non-zero depletion region in the poly electrode when the device operates in inversion ($V_{GS} > V_{TH}$).
 - This depletion region creates a capacitor in series with the gate oxide capacitor.
 - The MOS cap capacitance in inversion is smaller than in accumulation due to the poly depletion capacitance $C_{\text{polydepletion}}$.

MOS Models: Channel Inversion Charge

- Gate voltage values higher than the threshold voltage (V_{TH}) will result in an increase of the charge in the channel that is available for conduction.
 - We can define an effective gate-source voltage V_{eff} by:

$$V_{eff} \equiv V_{GS} - V_{TH}$$

- The charge density in the channel available for current conduction is proportional to V_{eff} and it is given by:

$$Q_n = C_{ox} \cdot V_{eff}$$

when $V_{DS} = 0$

MOS Models: I_D at low V_{DS}

- Current can be defined as the movement of a charge density Q_d (in C/m) with a velocity v (in m/s).

$$I = Q_d \cdot v$$

- Applying a very low drain bias relative to the source will cause carrier movement from source to drain through the channel without significant distortion of the channel inversion region.
 - For this approximation to hold $V_{DS} \ll 2 V_{eff}$

MOS Models: I_D at low V_{DS} (2)

- The resulting current between source and drain is:

$$I_D = -W \cdot Q_n \cdot v$$

where W is the transistor width,

$$Q_n = C_{ox} \cdot V_{eff}$$

$$v = \mu_n \cdot E$$

and E is the electric field in the channel that can be described by $E = -V_{DS} / L$ when V_{DS} has low values.

- Substituting and rearranging:

$$I_D = \mu_n \cdot C_{ox} \cdot W/L \cdot (V_{GS} - V_{TH}) \cdot V_{DS}$$

MOS Models: I_D at low V_{DS} (3)

- Important points to notice:
 - Increasing W (transistor width) will increase I_D because it is like adding extra channels in parallel.
 - Reducing L (transistor length) will increase I_D because the field across the channel is increased and hence the carrier velocity.
 - Increasing C_{ox} (gate capacitance) will increase I_D because more charge will be available for conduction in the channel.
 - Increasing μ_n (channel mobility) will increase I_D because the carriers will move "easier" in the channel with consequently higher velocity.
 - Increasing $V_{GS} - V_{TH}$ (gate effective bias) will increase I_D because more charge will be available in the channel for conduction.

MOS Models: Q_n along the channel

- Assuming the reference point being at the source edge of the channel, the charge along the channel Q_n can be described by:

$$Q_n(x) = C_{ox} \cdot [V_{GS} - V(x) - V_{TH}]$$

where $V(x)$ is the potential along the channel at a distance x from the source edge.

- The carrier velocity will be given by:

$$v(x) = \mu_n \cdot E(x) = \mu_n \cdot \left[-\frac{dV(x)}{dx} \right]$$

and the drain current I_D becomes:

$$I_D = W \cdot C_{ox} \cdot [V_{GS} - V(x) - V_{TH}] \cdot \mu_n \cdot \frac{dV(x)}{dx}$$

MOS Models: I_D in the triode region

- Integrating along the channel:

$$\int_{x=0}^L I_D \cdot dx = \int_{V=0}^{V_{DS}} W \cdot C_{ox} \cdot \mu_n \cdot \left[V_{GS} - V(x) - V_{TH} \right] \cdot dV$$

assuming that I_D is constant along the channel:

$$I_D \cdot x \Big|_{x=0}^L = W \cdot C_{ox} \cdot \mu_n \cdot \left[\left(V_{GS} - V_{TH} \right) \cdot V - \frac{V^2}{2} \right] \Big|_{V=0}^{V_{DS}}$$

$$I_D \cdot L = W \cdot C_{ox} \cdot \mu_n \cdot \left[\left(V_{GS} - V_{TH} \right) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_D = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot \left[\left(V_{GS} - V_{TH} \right) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

MOS Models: I_D in the triode region

- Drain current I_D presents a quadratic dependence with V_{DS} .
- At each value of $V_{GS} - V_{TH}$, the peak of the parabola is located at:

$$V_{DS} = V_{GS} - V_{TH}$$

with a resulting peak drain current of:

$$I_{D,\max} = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH})^2$$

MOS Models: I_D for $V_{DS} = (V_{GS} - V_{TH})$

- At this bias point, the channel “pinches-off” at the drain edge because the net gate bias to the channel at this location is:

$$V_{GD} = V_{GS} - V_{DS} = V_{TH}$$

- Any further increase of V_{DS} will not result in significant increase in drain current I_D . The transistor is said to be in saturation.

MOS Models: I_D analysis assumptions

- The I_D analysis that was presented assumes that:
 - The threshold voltage V_{TH} and the channel mobility μ_n are constant along the channel. Meaning that they don't vary with the distance from the source edge (x).
 - Moreover, V_{TH} and μ_n are considered to be independent of V_G and V_D .
- These assumptions are not always valid, leading to the addition of second-order effects to the model. We will discuss some of these effects later on in the class.

MOS Models: I_D equations

- At very low drain bias ($V_{DS} \ll 2 \cdot (V_{GS} - V_{TH})$)
 I_D has a linear dependence on V_{DS} .

$$I_D = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH}) \cdot V_{DS}$$

- At drain bias away from saturation ($V_{DS} \leq (V_{GS} - V_{TH})$)
 I_D has a quadratic dependence on V_{DS} .

$$I_D = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- At drain bias in saturation ($V_{DS} \geq (V_{GS} - V_{TH})$)
 I_D doesn't change with V_{DS}

$$I_D = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH})^2$$

MOS Models: Equivalencies

- The MOSFET in the linear region behaves as a resistor which value is determined by the gate bias.

$$\frac{V_{DS}}{I_D} = R_{on} = \frac{1}{\frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH})}$$

- In saturation the MOSFET can be described by a voltage controlled current source. The current dependence on the gate voltage is defined as the device transconductance g_m .

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}=cte} = \frac{\partial}{\partial V_{GS}} \left[\frac{1}{2} \cdot \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH})^2 \right]$$

MOS Models: Transconductances

- The transconductance in saturation is given by:

$$g_m = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH})$$

- A similar analysis can be used to calculate the g_m in the triode region ($g_{m,triode}$)

$$g_{m,triode} = \frac{\partial}{\partial V_{GS}} \left\{ \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right] \right\}$$

$$g_{m,triode} = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot V_{DS}$$

MOS Models: In Saturation for Amplification

- The transconductance linearly increases from zero with the device operating in the triode region until it reaches the saturation value determined by V_{eff} .
- The g_m value is maximum in saturation.
 - That is one of the reasons why MOSFETs are biased in saturation for amplification.

MOS Models: Alternate equations for g_m

- The transconductance in saturation g_m can also be calculated as:
 - The inverse of R_{on}
 - A function of I_D in saturation and V_{eff}

$$g_m = \frac{2 \cdot I_{D,sat}}{V_{GS} - V_{TH}}$$

MOS Models: 2nd order - L modulation

- I_D in saturation has a dependence on V_{DS} .
- The increase in V_{DS} results in a reduction of the effective channel as the point of channel pinch-off moves towards the source.
- The true channel length L' can be described by:

$$L' = L - \Delta L$$

where ΔL is proportional to the increase of the depletion region between the drain and the channel.

MOS Models: 2nd order - L modulation

- Defining λ as the channel-length modulation factor:

$$I_D = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS})$$

where: $\lambda \propto \frac{1}{L \cdot \sqrt{V_{DS}}}$

- The transconductance is also affected by λ and it is given by:

$$g_m = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH}) \cdot (1 + \lambda \cdot V_{DS})$$

MOS Models: L modulation

- Assuming all parameters the same and L modulation, the I_D vs. V_{DS} characteristics of NMOSFETs with L_1 and $L_2 = 2 \cdot L_1$ is:
 - A longer L gives a more ideal current source as the dependence with V_{DS} is minimized by the fact that $\lambda \propto 1/L$
 - This is achieved at the expense of a lower absolute current value.
 - W should be adjusted to provide the desired I_D

MOS Models: L Modulation

WARNING:

- The fact that $I_D \propto V_{DS}$ does NOT imply that the use of V_{DS} to set a desired I_D is a good approach.
- The dependence of I_D with V_{DS} is very WEAK.
- It is better to set I_D using V_{GS} and factor the effect of V_{DS} as an error.

MOS Models: Body Effect

- What happens if there is a bias between source and body?
 - The body bias affects the charge in the channel region causing a change in the threshold voltage.
- This happens because the gate needs to mirror the channel depletion charge Q_{d1} before it starts creating channel inversion charge.
- When the body is biased relative to the source, a higher depletion region is present in the channel and consequently the gate has to mirror a higher charge $Q_{d2} > Q_{d1}$ before the channel inversion starts.
- The net result is an increase on V_{TH} .

MOS Models: Body effect impacts V_{TH}

- The increase in V_{TH} due to the body bias is called body effect.
- The body effect coefficient γ is given by:

$$\gamma = \frac{\sqrt{2 \cdot q \cdot K_{Si} \cdot \epsilon_0 \cdot N_{SUB}}}{C_{ox}}$$

- Where, N_{SUB} is the substrate doping in the vicinity of the channel and $K_{Si} = 11.7$ is the dielectric constant of silicon.

MOS Models: V_{SB} changes V_{TH}

- Taking into account the body effect, the threshold voltage becomes:

$$V_{TH} = V_{TH0} + \gamma \cdot \left(\sqrt{2 \cdot \Phi_F + V_{SB}} - \sqrt{2 \cdot \Phi_F} \right)$$

where:
$$\Phi_F = \frac{k \cdot T}{q} \cdot \ln \left(\frac{N_{SUB}}{n_i} \right)$$

- Implications of the body effect:
 - The threshold voltage increases causing the reduction of the drain current I_D for a given gate bias V_{GS} .

MOS Models: V_{SB} notes

- The body effect can also appear if the source potential is varied and the body potential is kept constant.
- It is the potential between source and body V_{SB} that causes the body effect.
- The body effect is usually undesirable.
- The change in V_{TH} complicates the circuit design.
- Usually, N_{SUB} and C_{ox} are defined to minimize γ

MOS Models: Body effect example

- Example: Constant I_D with:
 - A) Body tied to source, $V_{SB} = 0$
 - B) Body tied to ground, $V_{SB} = V_S$

MOS Models: Subthreshold Operation

- At $V_{GS} \approx V_{TH}$ a weak inversion layer exists in the channel and current flows from source to drain.
- Even for $V_{GS} < V_{TH}$ a finite drain current I_D exists. This is called subthreshold conduction.
- An exponential current-voltage dependence exists, and it is given by:

$$I_D = I_0 \cdot \exp\left(\frac{V_{GS}}{\zeta \cdot \frac{k \cdot T}{q}}\right)$$

where $\zeta > 1$ is a non-ideality factor.

MOS Models: Subthreshold Slope

- The subthreshold slope (S) is defined by the voltage change required to cause a variation of one decade in the drain current.
 - Typical values of S are between 70mV/dec and 100mV/dec.
- A smaller value of the subthreshold slope indicates that the device requires a smaller change in V_{GS} to switch on and off.
- The exponential dependence of I_D with V_{GS} might cause erroneous expectations of high gain.
 - This relationship is only valid in a regime where the device has low I_D , severely limiting the usefulness of devices operating in the subthreshold regime.

MOS Models: Device Capacitances

- A capacitance exists between every two terminals of the MOS device.
 - C_{GD} , C_{GS} , C_{GB} , C_{DB} , C_{SB}

- The capacitances are derived from the device structure.

MOS Models: Structure Capacitances

- Capacitance between gate and the channel across the gate oxide.

$$C_1 = W \cdot L \cdot C_{ox}$$

- Capacitance between the channel and the substrate across the depletion region.

$$C_2 = W \cdot L \cdot \sqrt{\frac{q \cdot K_{Si} \cdot \epsilon_0 \cdot N_{SUB}}{4 \cdot \Phi_F}}$$

- Capacitance between the gate and the source and drain across the overlap regions and due to fringing fields.

$$C_3 = C_4 = W \cdot C_{ov}$$

MOS Models: Junction Capacitances

- Capacitance between source and drain and the substrate.
 - These are usually decomposed in bottom plate junction capacitance and sidewall capacitance.

$$C_5 = W \cdot L \cdot C_{jd} + 2 \cdot (W + L) \cdot C_{jswd}$$

$$C_6 = W \cdot L \cdot C_{js} + 2 \cdot (W + L) \cdot C_{jsws}$$

where:

$$C_{jd} = \frac{C_{jo}}{\sqrt{1 + \frac{V_{DB}}{\Phi_o}}}$$

$$C_{jswd} = \frac{C_{jsw0}}{\sqrt{1 + \frac{V_{DB}}{\Phi_o}}}$$

$$C_{js} = \frac{C_{jo}}{\sqrt{1 + \frac{V_{SB}}{\Phi_o}}}$$

$$C_{jsws} = \frac{C_{jsw0}}{\sqrt{1 + \frac{V_{SB}}{\Phi_o}}}$$

$$\Phi_o = \frac{k \cdot T}{q} \cdot \ln \left(\frac{N_A \cdot N_D}{n_i^2} \right)$$

MOS Models: Device Capacitances

- The device capacitances vary with the device operation point.
- With the device OFF

$$C_{GD} = C_{GS} = W \cdot C_{ov}$$

$$C_{GB} = \frac{W \cdot L \cdot C_{ox} \cdot C_2}{W \cdot L \cdot C_{ox} + C_2}$$

- In the Triode region

- The gate to channel capacitance is equally split between source and drain, as a change in V_{GS} draws equal charge from source and drain.

$$C_{GD} = C_{GS} = \frac{W \cdot L \cdot C_{ox}}{2} + W \cdot C_{ov}$$

- C_{GB} is neglected due the channel shielding effect.

MOS Models: Saturation capacitances

- Due to the channel pinch-off C_{GD} is not affected by the channel.

$$C_{GD} = W \cdot C_{ov}$$

- The source is still tied to the channel and:

$$C_{GS} = \frac{2}{3} \cdot W \cdot L \cdot C_{ox} + W \cdot C_{ov}$$

- The channel continues to shield the gate from the substrate and C_{GB} is neglected.

MOS Models: Isolation impact on cap

- Transistor in the well: the case that we used.
- Single transistor with Shallow Trench Isolation.
 - Eliminates sidewall component.
- Single transistor made on Silicon-on-Insulator.
 - Eliminates ALL junction capacitances.

MOS Models: Small-signal model

- In most analog circuits MOS devices are biased in the saturation (active) region.
- The small-signal model describes the device operation around the bias point.
 - It is derived by applying a small variation to one of the bias points and calculating the effect on the other bias parameters.
- Variation on V_{GS} will result in variation on I_D .
 - This can be described by a voltage-controlled current source equal to:

$$I_d = g_m \cdot V_{gs}$$

where:

$$g_m = \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH})$$

MOS Models: Small-signal model

- Variation on V_{DS} will result in variation on I_D due to the channel length modulation.
 - This can also be described by a voltage-controlled current source. However, a current source whose value of current linearly depend on the voltage across it, can be described by a resistance.

$$r_o = \frac{\partial \mathcal{N}_{DS}}{\partial I_D} = \frac{1}{\frac{\partial I_D}{\partial \mathcal{N}_{DS}}} = \frac{1}{\frac{1}{2} \cdot \frac{W}{L} \cdot \mu_n \cdot C_{ox} (V_{GS} - V_{TH})^2 \cdot \lambda}$$

$$r_o = \frac{1}{\lambda \cdot I_D}$$

MOS Models: Small-signal model

- Variation on V_{BS} will affect I_D through the body effect.
 - This is modeled by a voltage-controlled current source given by:

$$I_d = g_{mb} \cdot V_{bs}$$

where:

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\partial I_D}{\partial V_{TH}} \cdot \frac{\partial V_{TH}}{\partial V_{BS}}$$

$$g_{mb} = -\frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{GS} - V_{TH}) \cdot \frac{-\gamma}{2 \cdot \sqrt{V_{SB} + 2 \cdot |\Phi_F|}}$$

$$g_{mb} = \frac{g_m \cdot \gamma}{2 \cdot \sqrt{V_{SB} + 2 \cdot |\Phi_F|}}$$

MOS Models: Small-signal model

- Schematic of NMOSFET small-signal model.

MOS Models: SPICE Nuts and Bolts

- Circuit simulator that solves the nodal equations associated to the circuit.
- The circuit components are described by models.
- The model parameters for each circuit component need to be set to the desired values.
- Usually, the model parameters are specified by the foundry or fabrication facility that will make the chips.

It is very unusual for the designers to be able to modify the model parameters away from the factory specifications.

MOS Models: SPICE circuit description

- Label all the nodes in the circuit.
 - The ground is always numbered 0 (zero).
- Identify all the voltage and current sources
- Identify the model to be used for each device.
 - How many distinct device types are being used?
- Create a "net list" that describes the circuit.

MOS Models: SPICE component definition

- Different models for each distinct device type.
 - Existing models are organized in complexity levels.
 - Level 1 is the simplest, Level 3 is the most complex.
- Typical MOS device model parameters are:
 - VTO Threshold voltage (V)
 - UO Carrier mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)
 - TOX Gate oxide thickness (m)
 - GAMMA Body effect parameter γ
 - LAMBDA Channel length coefficient λ (1/V)
 - CJ Bottom plate junction capacitance (F/m^2)
 - CJSW Sidewall junction capacitance (F/m)
 - CGDO Gate-drain overlap capacitance (F/m)
 - CGSO Gate-source overlap capacitance (F/m)
 - LD Lateral diffusion of junction under gate (m)

MOS Models: SPICE parameter values

- As fabrication technology changes the parameters that describe the MOS devices changes.

<u>Parameter</u>	<u>0.8μm Tech</u>	<u>0.5μm Tech</u>
VTO	n 0.7: p -0.9	n 0.7: p -0.8
UO	n 500: p 175	n 350: p 100
TOX	1.8×10^{-8}	9×10^{-9}
GAMMA	n 0.5: p 0.8	n 0.45: p 0.4
LAMBDA	n 0.1: p 0.2	n 0.1: p 0.2
CJ	n 2.5×10^{-4} : p 4×10^{-4}	n 5.6×10^{-3} : p 9.4×10^{-3}
CJSW	n 2×10^{-10} : p 2.8×10^{-10}	n 3.5×10^{-11} : p 3.2×10^{-11}
CGDO		n 4×10^{-10} : p 3×10^{-10}
CGSO		n 4×10^{-10} : p 3×10^{-10}
LD	6×10^{-8}	n 8×10^{-8} : p 9×10^{-8}