
EE5321/EE7321

Semiconductor Devices and Circuits

Op Amps - Part1

High gain amps for negative feedback

- The need for High-Gain-Amplifiers is related to the concept of feedback and the requirement for having precisely defined transfer functions in analog circuits

- With:

$x \rightarrow$ current or voltage signals

$A \rightarrow$ the high gain amplifier

$F \rightarrow$ the feedback network

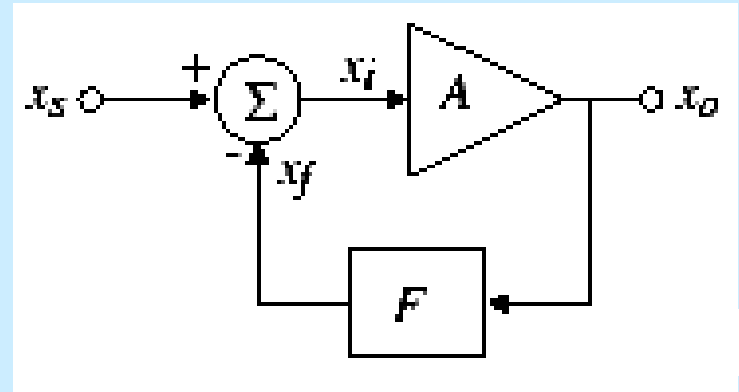
- The closed loop gain is:

$$A_f = \frac{x_o}{x_s} = \frac{A}{1 + A \cdot F}$$

- If A is very large $\rightarrow A \cdot F \gg 1$ and consequently:

$$A_f = \frac{x_o}{x_s} \approx \frac{1}{F} \quad \rightarrow$$

The overall gain is defined by the feedback network



Types of amplifiers

- The gain of the High-Gain amplifier stage is:

$$A = x_o/x_i$$

- Since x can be a voltage or current signal, there are four types of amplifiers

Types of Amplifiers	Voltage-controlled, current-source	Voltage-controlled, voltage-source	Current-controlled, current-source	Current-controlled, voltage-source
x_i variable*	Voltage	Voltage	Current	Current
x_o variable	Current	Voltage	Current	Voltage
Desired R_i	Large	Large	Small	Small
Desired R_o	Large	Small	Large	Small

* The x_i , x_s , and x_f must all be the same type of variable, voltage or current.

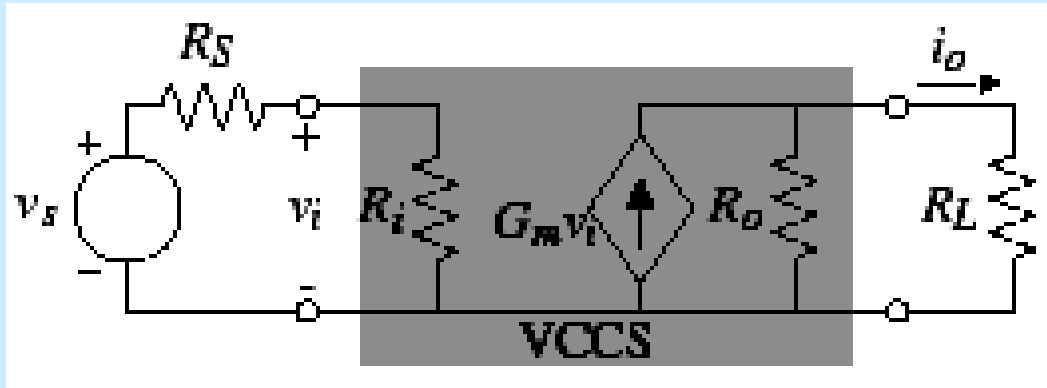
- The variables x_i , x_s and x_f must all be the same type of variable, voltage or current

Architectures for High Gain Amps

- Architectures provide the starting point for the selection of the building blocks when designing high gain amplifiers.
- As optimization proceeds the boundaries between stages become fuzzy.
- The advantage of using an architecture viewpoint is that it identifies the generic elements of the design.
- Designs that start from the same architecture can have a completely different final version.

Voltage controlled current source amp

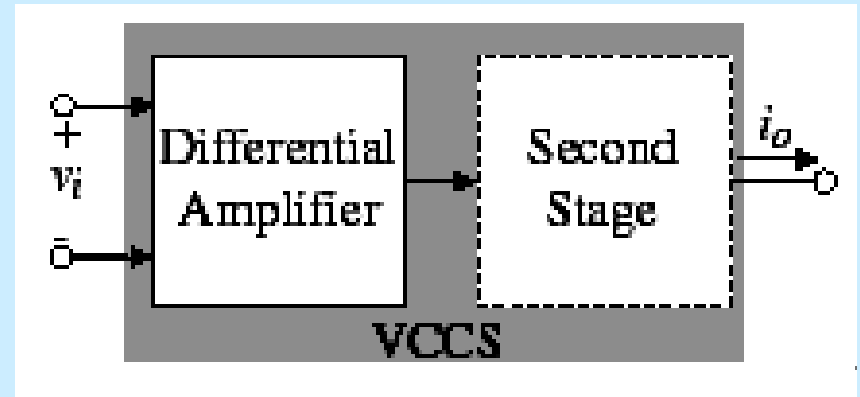
- Also called *Operational Transconductance Amp (OTA)*



- Large $R_i \rightarrow \infty$
- Large $R_o \rightarrow \infty$
- $G_M \rightarrow G_m$

$$\frac{i_o}{v_s} = G_M = \frac{G_m \cdot R_o \cdot R_i}{(R_i + R_s) \cdot (R_o + R_L)}$$

- Diff Amp:
 - High R_i , good Gain
- Second Stage:
 - Increase R_o , more Gain

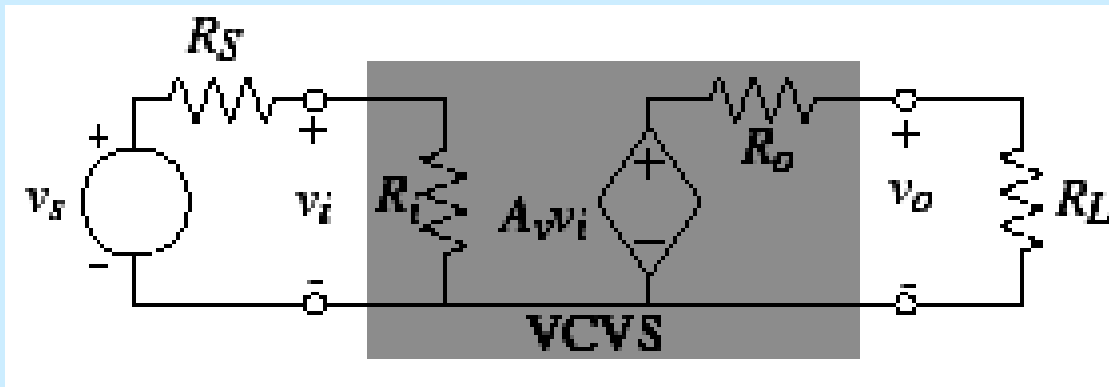


Voltage controlled voltage source amp

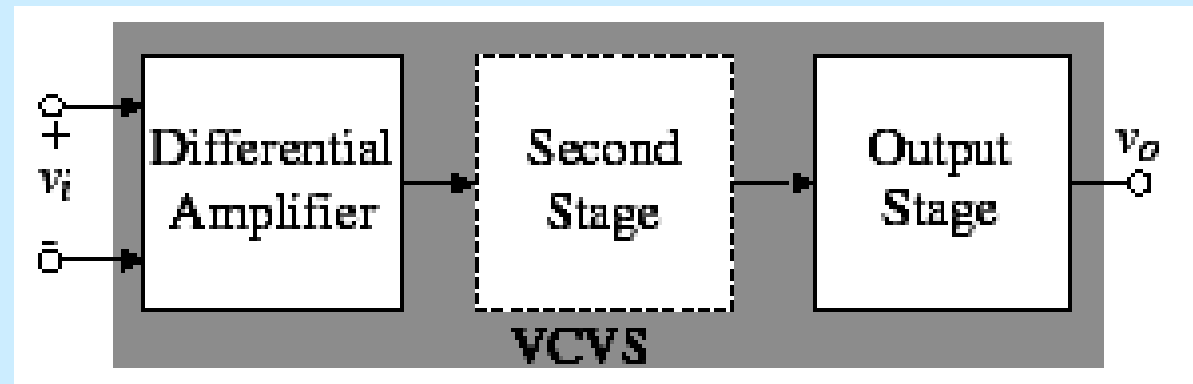
- Also called *Operational Amplifier*

$$\frac{v_o}{v_s} = A_V = \frac{A_v \cdot R_i \cdot R_L}{(R_i + R_S) \cdot (R_o + R_L)}$$

- Large $R_i \rightarrow \infty$
- Small $R_o \rightarrow 0$
- $A_V \rightarrow A_v$



- Output Stage:
 - Lower R_o

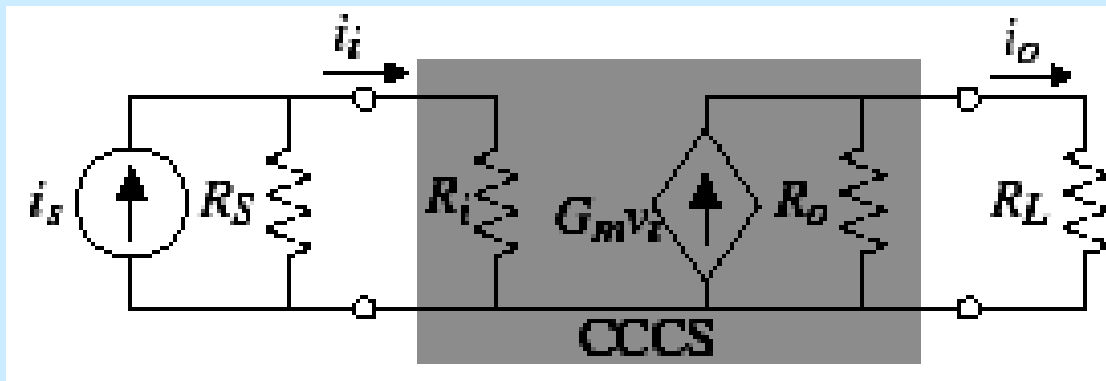


Current controlled current source amp

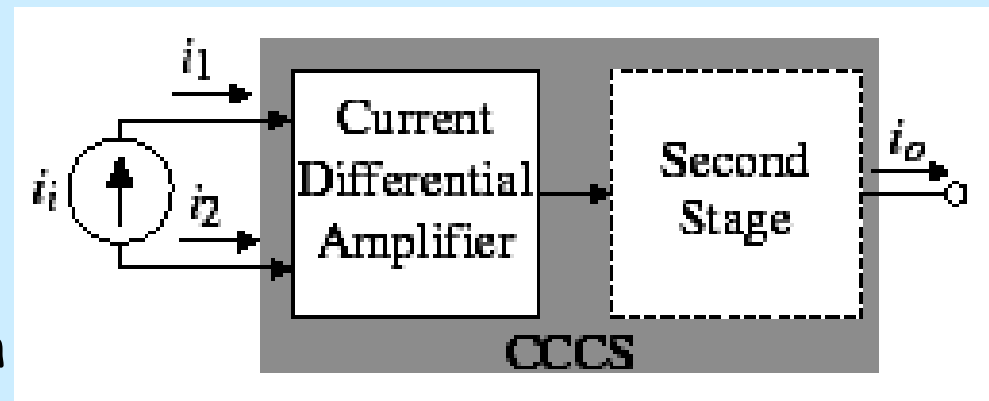
- Require a current driven input with small R_i

$$\frac{i_o}{i_s} = A_I = \frac{A_i \cdot R_S \cdot R_o}{(R_i + R_S) \cdot (R_o + R_L)}$$

- Small R_i ($\rightarrow 0$)
- Large R_o ($\rightarrow \infty$)
- $A_I \rightarrow A_i$



- Current Diff Amp:
 - Small R_i , Small Gain
- Second Stage:
 - Increase R_o , more Gain

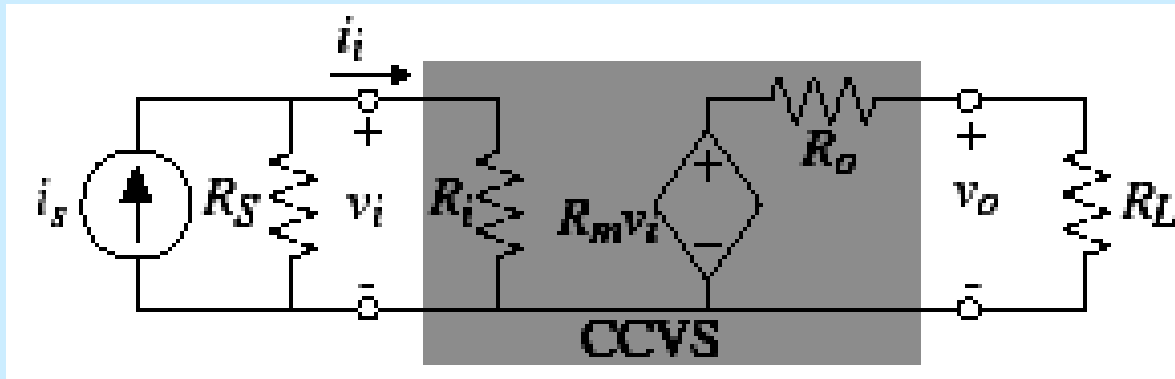


Current controlled voltage source amp

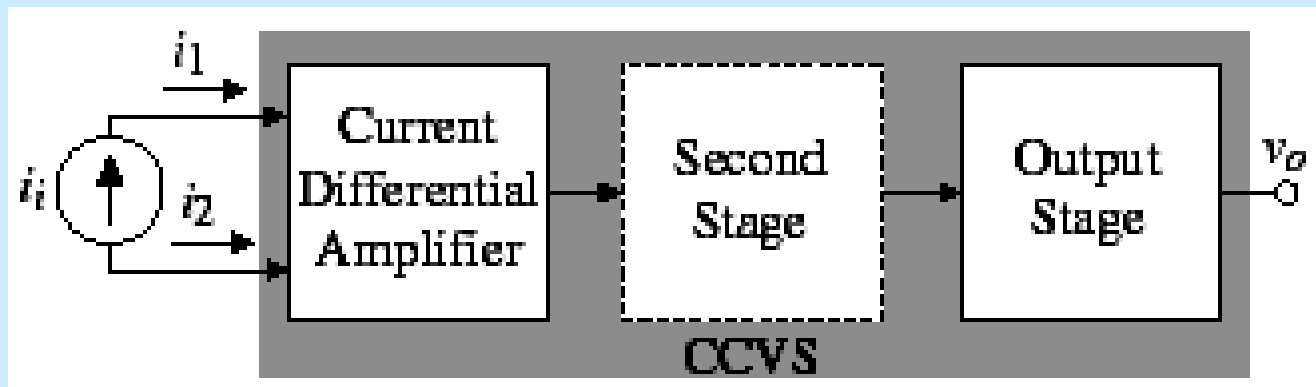
- Also uses a current driven input with small R_i

$$\frac{V_o}{i_s} = R_M = \frac{R_m \cdot R_S \cdot R_L}{(R_i + R_S) \cdot (R_o + R_L)}$$

- Small $R_i \rightarrow 0$
- Small $R_o \rightarrow 0$
- $R_M \rightarrow R_m$

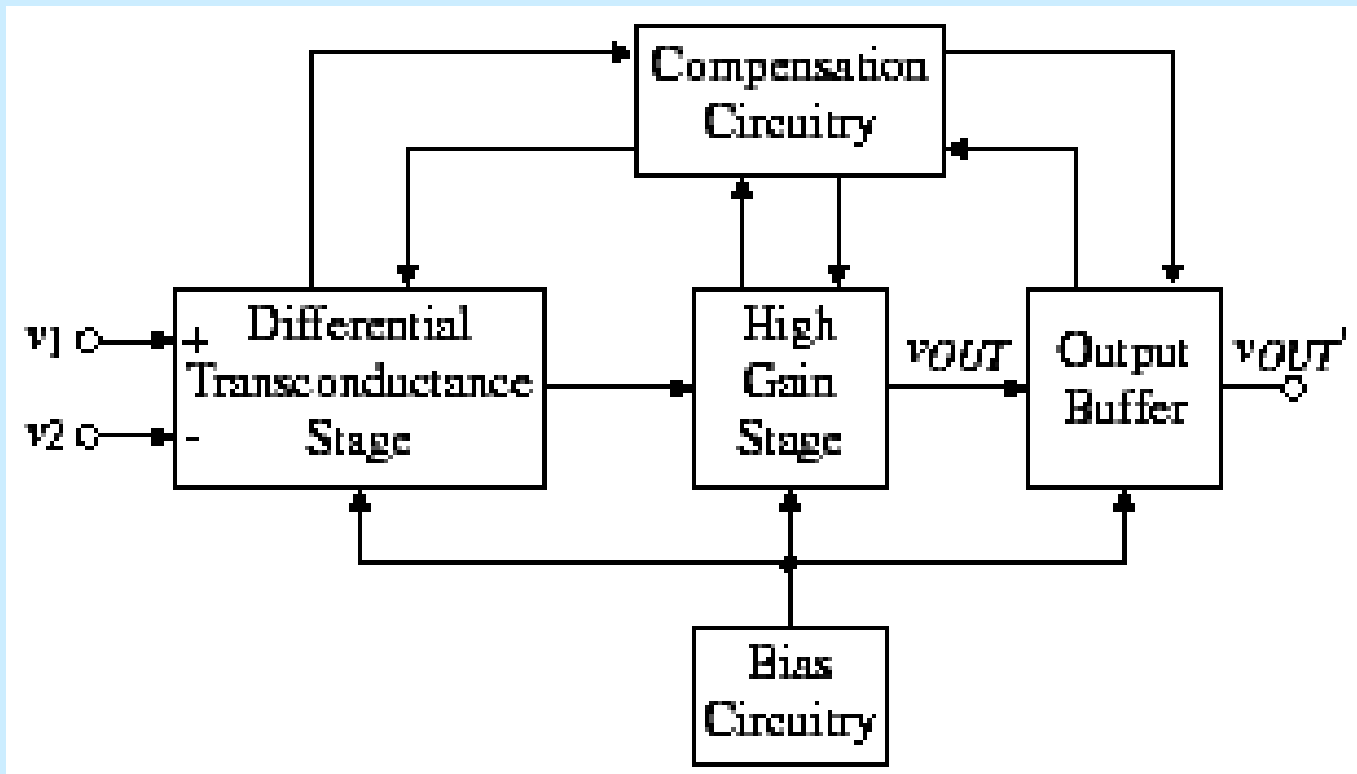


- Second Stage:
 - More Gain
- Output Stage:
 - Lower R_o



Block diagram general two-stage Op Amp

- Differential input: Gain, noise performance
 - High Gain Stage might be added to increase Gain
- Output buffer needed to drive small load
- Bias circuit assure proper bias point across circuit



Ideal Op Amp

- Gain $A_v \rightarrow \infty$ $R_{in} \rightarrow \infty$ $R_{out} \rightarrow 0$

- If we define:

$$v_i = v_1 - v_2$$

$$i_i = i_1 - i_2$$

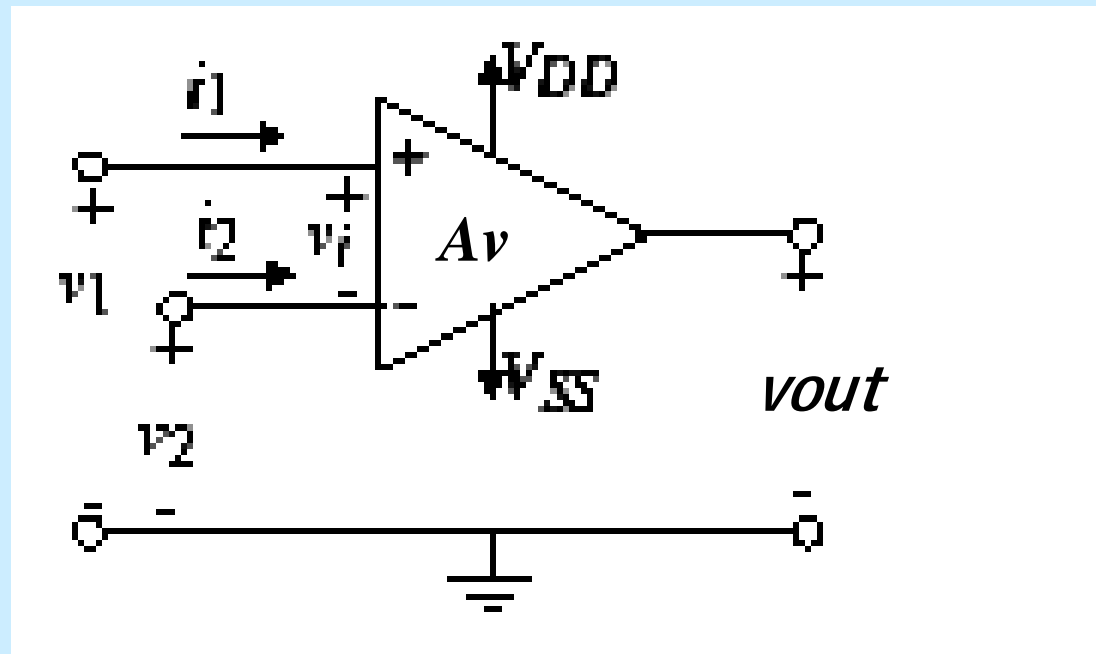
- And we have:

$$v_{OUT} = A_v \cdot (v_1 - v_2)$$

- Then:

$$v_i = i_i = 0$$

when negative feedback is applied (null port).



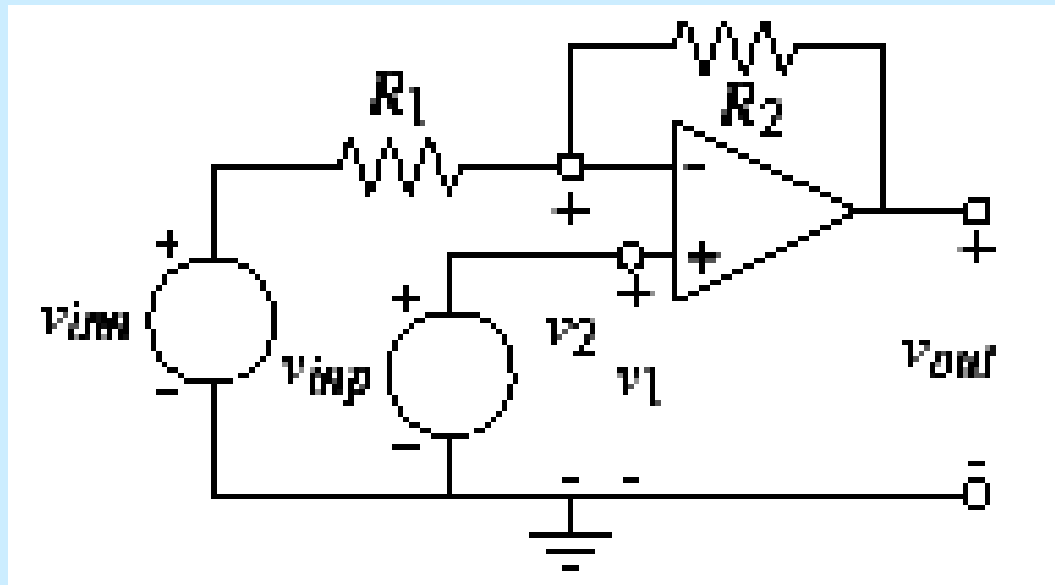
General voltage amplifier configuration

- Non-inverting voltage amplifier ($v_{inn} = 0$):

$$v_{out} = \left(\frac{R_1 + R_2}{R_1} \right) \cdot v_{inp}$$

- Inverting voltage amplifier ($v_{inp} = 0$):

$$v_{out} = - \left(\frac{R_2}{R_1} \right) \cdot v_{inn}$$



Simple Voltage Amp with Op Amp

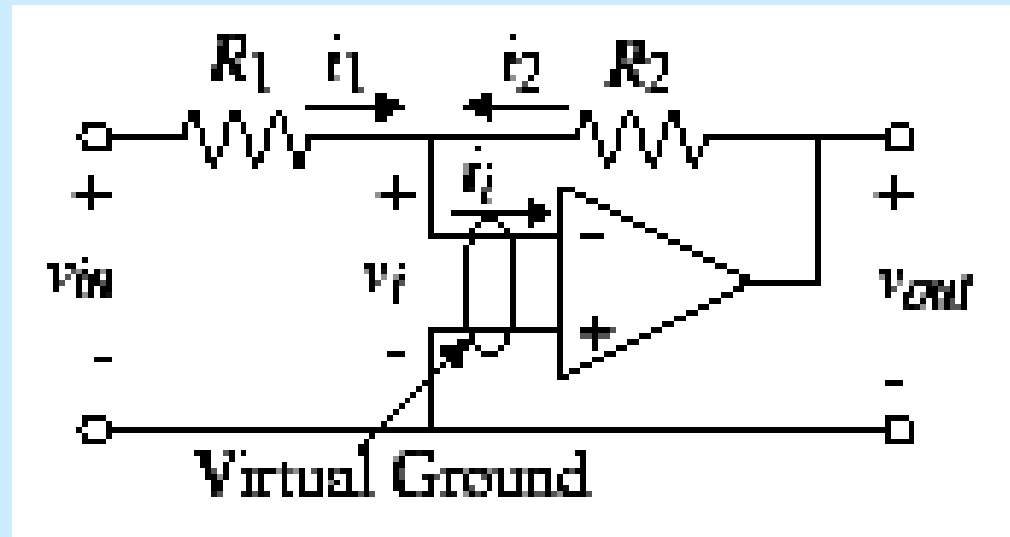
- Inverting voltage amplifier using Op Amp
 - Assuming that the voltage gain A_v is large enough, v_i and i_i are equal to zero

$$i_1 = \frac{V_{in}}{R_1}$$

$$i_2 = \frac{V_{out}}{R_2}$$

$$i_1 + i_2 = 0$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$



Op Amp Non-Idealities

R_{id} = differential input resistance

C_{id} = differential input capacitance

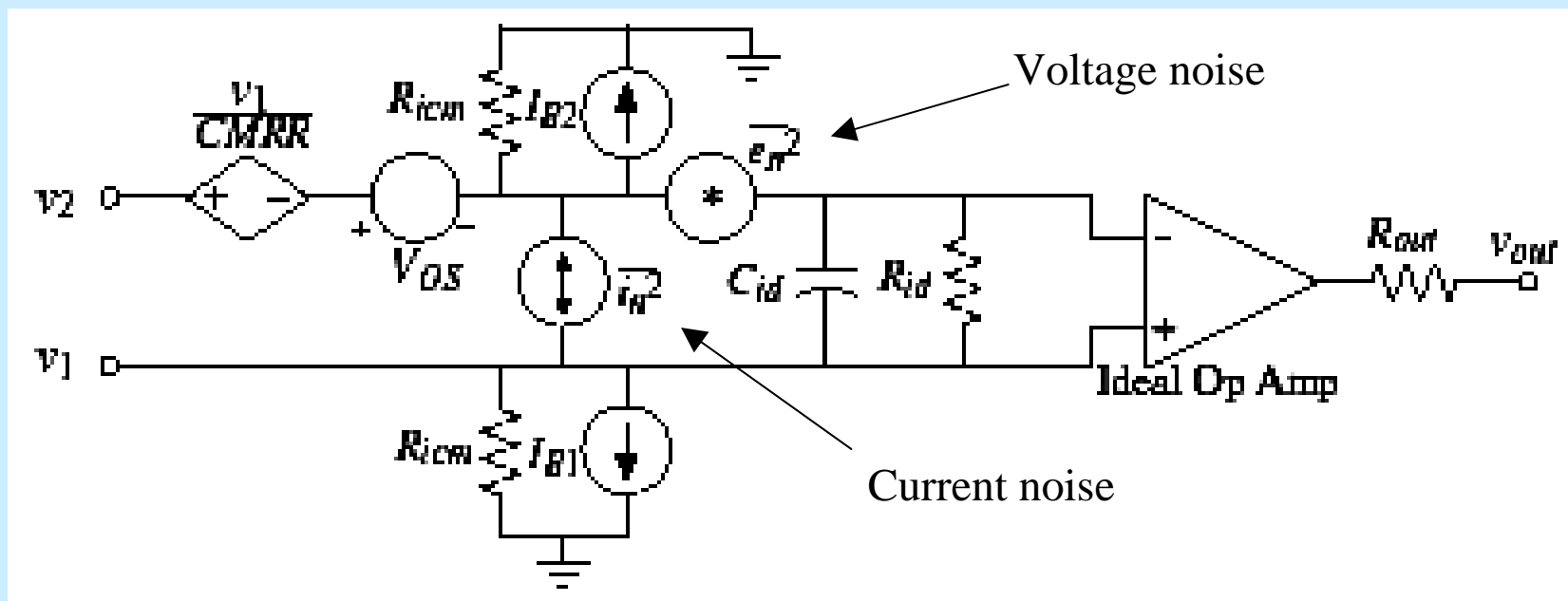
R_{icm} = common mode input resistance

V_{OS} = input offset voltage

I_{B1} and I_{B2} = differential input bias currents

I_{OS} = input offset current ($I_{OS} = I_{B1} - I_{B2}$)

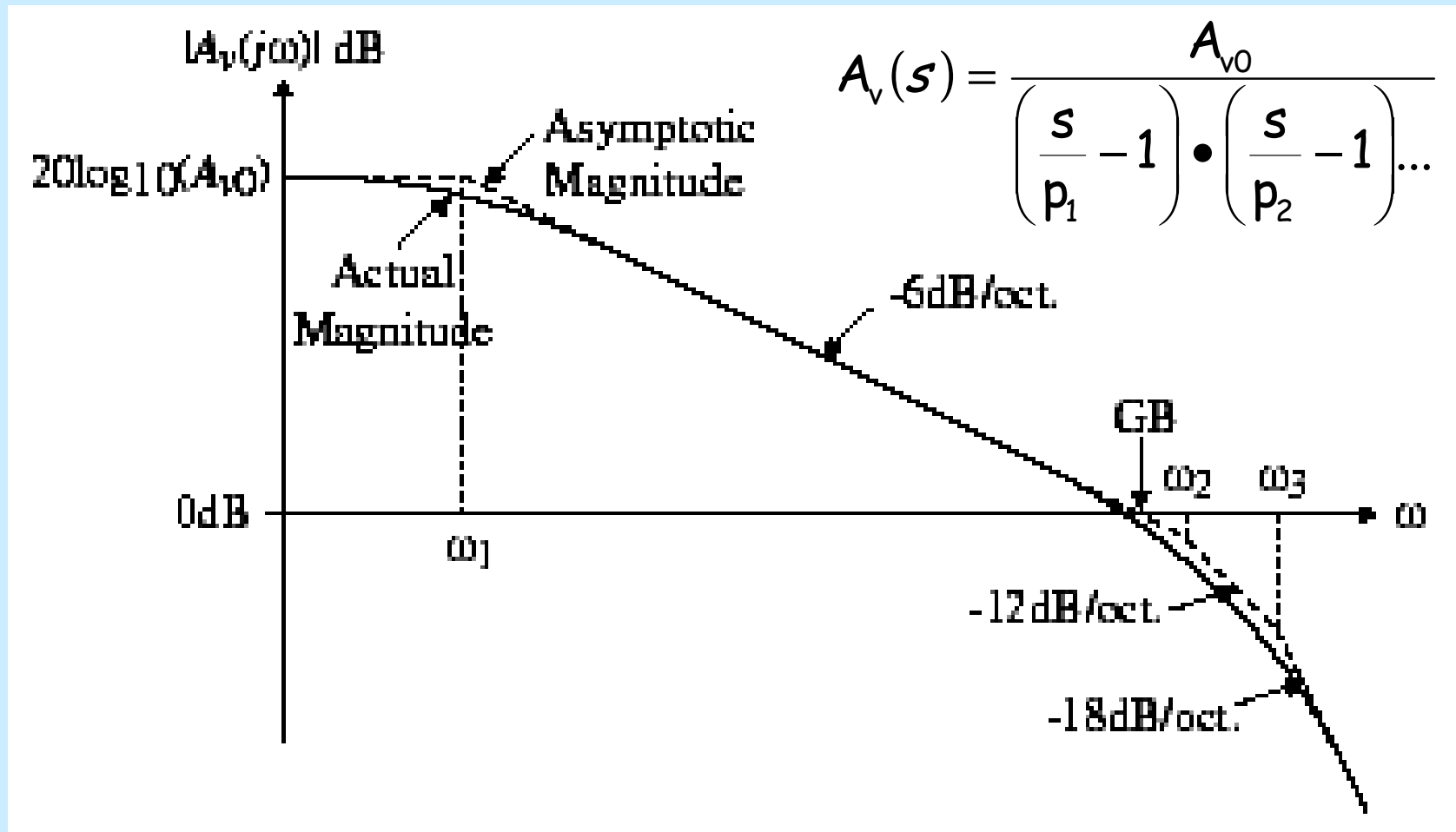
CMRR = Common Mode Rejection Ratio



Differential Frequency Response

- Differential and Common mode frequency response

$$V_{\text{out}}(s) = A_v(s) \cdot [V_1(s) - V_2(s)] \pm A_c(s) \cdot \left(\frac{V_1(s) + V_2(s)}{2} \right)$$



Power Supply Rejection Ratio

- PSSR is defined as the product of the open loop gain (A_v) and the ratio of the change in supply voltage to the corresponding change caused in the output voltage.

$$\text{PSSR} = \frac{\Delta V_{DD}}{\Delta V_{OUT}} \cdot A_v = \frac{v_{out}/v_{in} (v_{dd} = 0)}{v_{out}/v_{dd} (v_{in} = 0)}$$

- By defining A^+ and A^- as the small signal gain from the positive and negative power supplies to the output, respectively we can have:

$$\text{PSSR}^+ = \frac{A_{dm}}{A^+} \qquad \text{PSSR}^- = \frac{A_{dm}}{A^-}$$

I CMR and CMRR

- ICMR (Input Common Mode Range) is the voltage range over which the input common mode signal can vary without influencing the differential performance.
- CMRR (Common Mode Rejection Ratio) indicates the impact of the common mode signal on the differential output. It can also be regarded as the change in the input offset voltage that result from a unit change in the common mode input voltage.

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|$$

$$v_o = A_{dm} \cdot v_{id} + A_{cm} \cdot v_{ic}$$

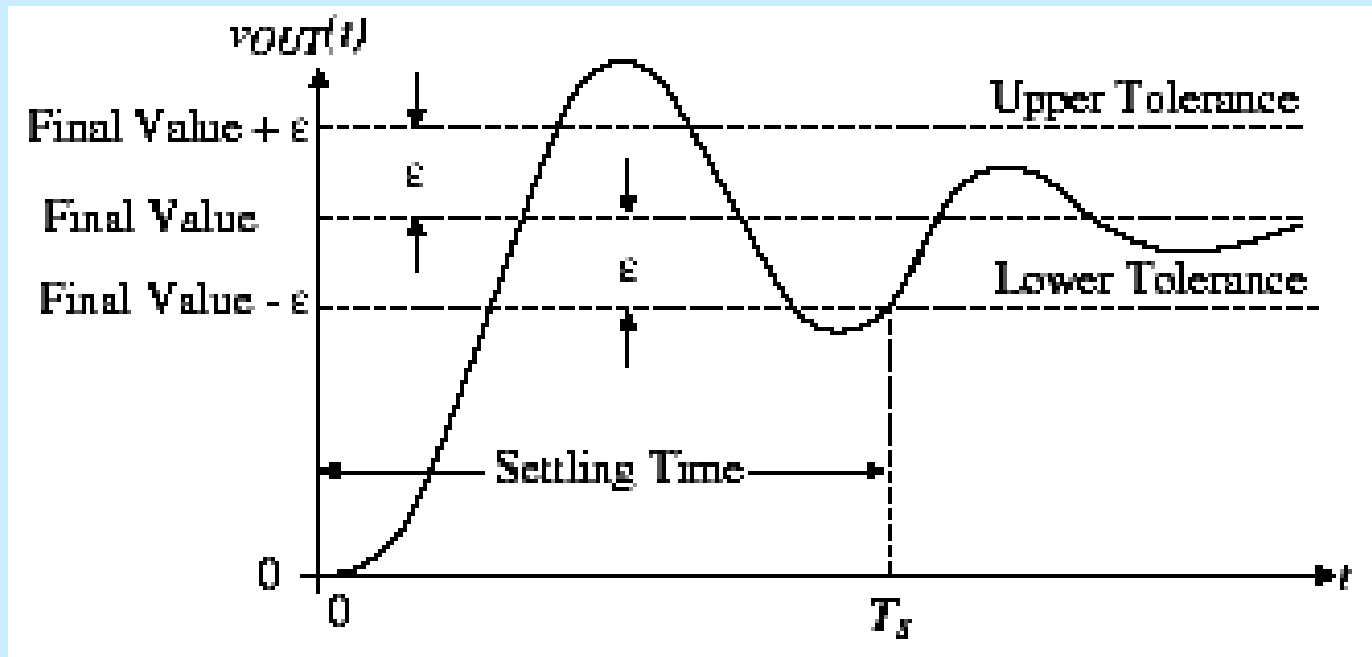
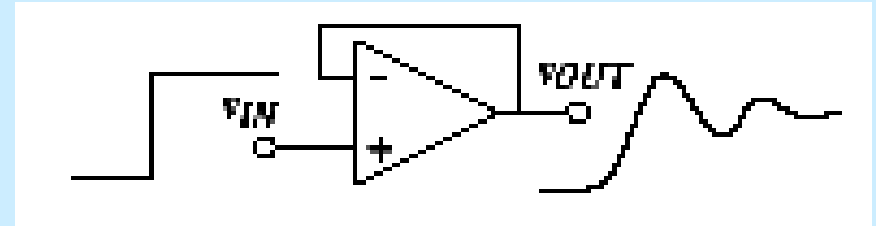
$$v_o = A_{cm} \cdot \Delta V_{ic} = \Delta V_o$$

$$v_{id,offset} = \Delta V_{id} = \Delta V_o / A_{dm}$$

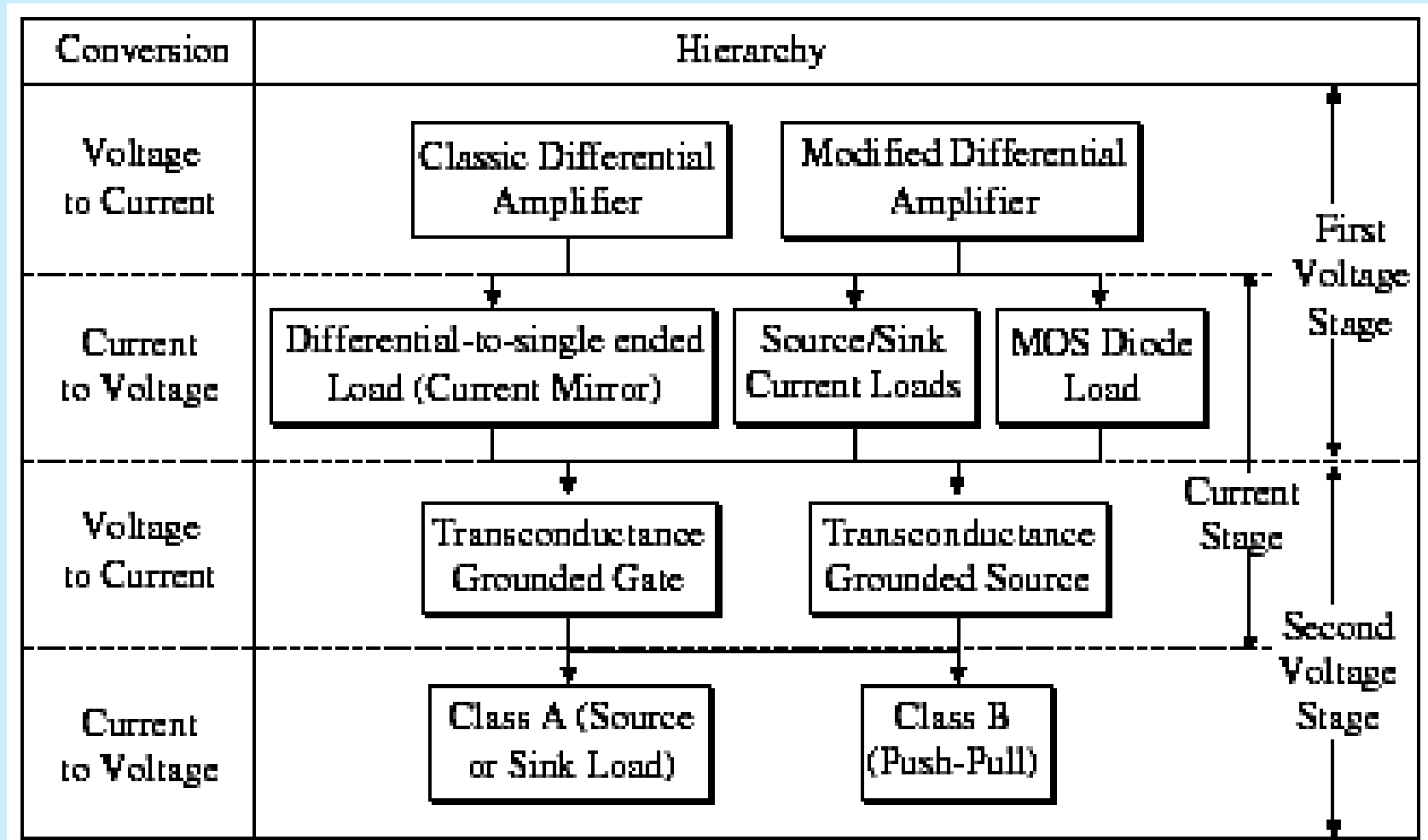
$$\Delta V_{id,offset} = \Delta V_{ic} / CMRR$$

Op Amp Settling Time

- T_s is the time needed for the output of the Op Amp to reach a value within the set tolerance when excited by a small signal

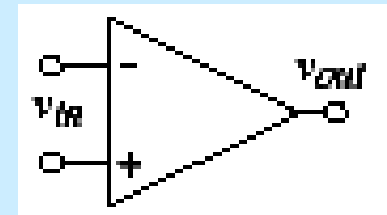
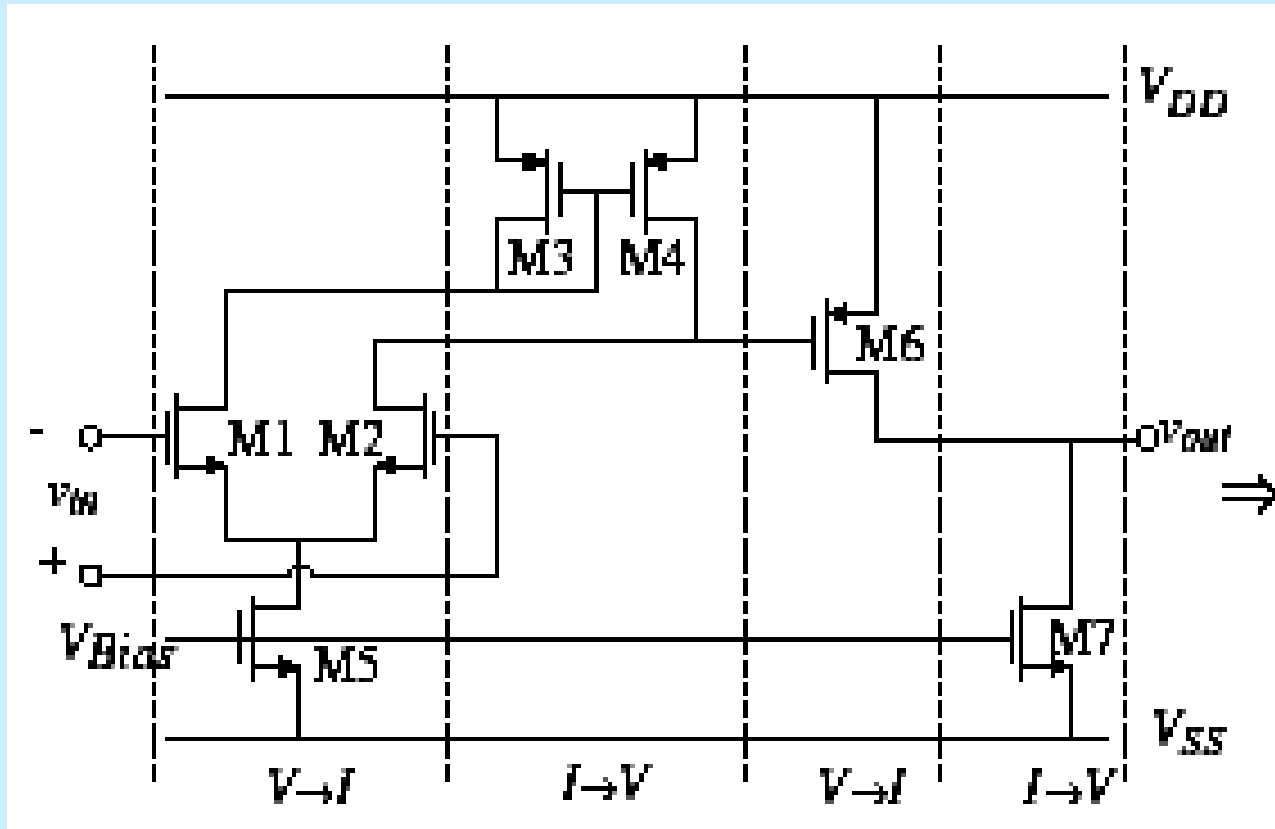


Signal path in CMOS Op Amps



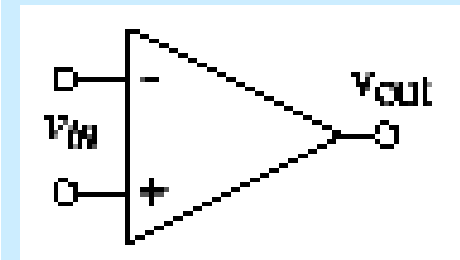
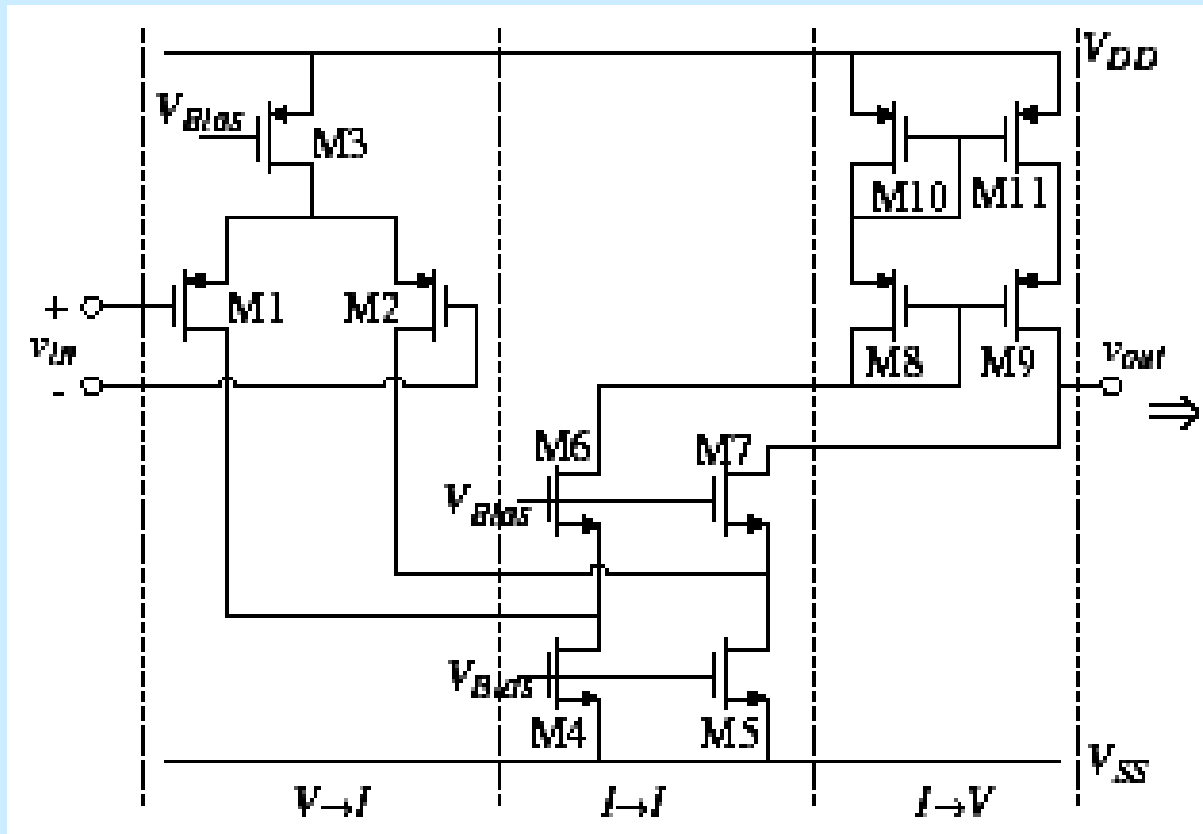
Two-stage CMOS Op Amp

- Classical two-stage CMOS Op Amp showing the changes in the signal.



Folded Cascode CMOS Op Amp

- Improves the input common-mode range and the PSRR of the two-stage op amp.
- It has a push-pull output instead of a Class A



Design of CMOS Op Amps

- Choose/Create the basic structure of the Op Amp
 - A diagram showing the various transistors and their interconnects results.
 - In general, this structure does not change during the next steps of the design.
- Selection of the DC currents and x tor sizes
 - Biggest portion of the design.
 - Computer simulations are used to verify hand calculations.
 - The compensation circuit is also designed during this step.
- Physical implementation of the design
 - Layout of the x tors and floorplanning
 - Resolve the parasitics and validate the layout
- Fabrication
- Measurement

Practical aspects of CMOS op amp design

- Decide upon a suitable configuration
 - It should be one capable of meeting most of the specs.
 - Start with existing topologies. Avoid inventing a new one.
 - Experience helps a lot in this stage.
- Determine the type of compensation needed
 - Consider the load and stability requirements.
 - Use some form of Miller or self-compensation approach.
- Design the device sizes for proper DC, AC and Transient performance
 - Start with hand calculations using approximate equations.
 - The compensation components are also sized in this step.
 - Use a circuit simulator to check and tune the design
- Useful rule in Analog Design (P.E. Allen book)
 - (use of simulator) \times (common sense) = Constant

Boundary conditions and requirements

- Typical Boundary Conditions (Unbuffered)
 - Process specifications (V_{ts} , k 's, C_{ox} , etc...)
 - Supply voltage and range $\pm 2.5V \pm 10\%$
 - Supply current and range $100\mu A$
 - Operating Temperature and range 0 to $70^\circ C$
- Requirements
 - Gain value and Gain Bandwidth $\geq 70dB$ $\geq 5MHz$
 - Slew rate and Settling Time $\geq 5V/\mu s$ $\leq 1\mu s$
 - Common-mode input range, ICMR $\geq \pm 1.5V$
 - Common-mode rejection ratio, CMRR $\geq 60dB$
 - Power supply rejection ratio, PSRR $\geq 60dB$
 - Output voltage swing $\geq \pm 1.5V$
 - Output resistance N/A, capacitive load
 - Offset $\leq \pm 10mV$
 - Noise $\leq 100nV/\sqrt{Hz}$ at $1KHz$
 - Layout Area $\leq 10^4 \times L_{min}$

References

- Gray (text book): 6.1 - 6.7